

Serial No.: 10/015,757  
Atty. Docket No.: P67358US0

**IN THE CLAIMS:**

Please cancel/amend/retain/add the claims as follows:

1. (Currently Amended) A semiconductor device comprising:

a plurality of metal wire patterns, each of said plurality of metal wire patterns  
including,

at least one pad pattern; which include

a fine line pattern having a width of less than 1  $\mu\text{m}$ ; and

at least one connection pad pattern for electrically connecting the pad  
pattern to the fine line pattern;

said pad pattern, said fine line pattern and said connection pad pattern of  
each of said plurality of metal wire patterns being formed in one layer, pad patterns, said plurality  
of metal wire patterns being formed by patterning a same layer and being electrically connected  
to each other, an area of the fine line pattern being formed to be more than 1% of a total area of  
said plurality of metal wire patterns for preventing corrosion of the fine line pattern from a  
chemical-mechanical polishing process and a width of said connection pad pattern being in a  
range between a width of said pad pattern and the width of said fine line pattern.

2. (Canceled).

3. (Canceled).

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4. (Previously Presented) The semiconductor device as recited in claim 1, wherein the plurality of metal wire patterns are made of aluminum or copper.

5. (Currently Amended) A semiconductor device for preventing corrosion of metal wires from a chemical mechanical polishing process, comprising:

a plurality of metal wire patterns, each of said plurality of metal wire patterns including, which include

main fine line patterns having a width of less than  $1\text{ }\mu\text{m}$ ;

main pad patterns;

connection pad patterns for electrically connecting said pad patterns to said main fine line patterns; and

dummy fine line patterns having a sub-micron width; ~~said plurality of metal wire patterns being formed by patterning a same layer,~~

said pad patterns, said fine line patterns and said connection pad patterns of each of said plurality of metal wire patterns being formed in one layer, an area of the dummy fine line patterns, which are connected to the pad patterns, being formed to be less than 1% of a total area of said plurality of metal wire patterns and also being less than a value obtained by dividing an area of the main fine line patterns by said total area and a width of said connection pad patterns being in a range between a width of said main pad patterns and the width of said main fine line patterns.

6. (Original) The semiconductor device as recited in claim 5, wherein the dummy fine line patterns are formed parallel with the main fine line patterns at a distance of a width of the main fine line pattern.

7. (Previously Presented) The semiconductor device as recited in claim 5, wherein the plurality of metal wire patterns are made of aluminum or copper wire.

8. (Previously Presented) The semiconductor device as recited in claim 5, wherein the dummy fine line patterns do not form or contribute to any electric circuit.

9. (Canceled)

10. (Previously Presented) The semiconductor device as recited in claim 5, wherein the plurality of metal wire patterns further include dummy pad pool patterns, to which the dummy fine line patterns are connected, said dummy pad pool patterns and said dummy fine line patterns being electrically disconnected from the main fine line patterns and the main pad patterns.

11. (Canceled).

12. (Previously Presented) The semiconductor device as recited in claim 5, wherein the plurality of metal wire patterns further include connection pad patterns which electrically connect the main pad patterns to the fine line patterns, said connection pad patterns being included in said total area.

13. (Previously Presented) The semiconductor device as recited in claim 12, wherein the total area is represented by  $A_p + A_c + A_d$ , where, 'd' represents the area of the dummy fine line patterns, 'A<sub>p</sub>' represents an area of the main pad patterns, 'A<sub>c</sub>' represents an area of the connection pad patterns and 'A' represents the area of the main fine line patterns.

14. (Canceled).

15. (Currently Amended) A semiconductor device for preventing corrosion of aluminum or copper wires from a chemical mechanical polishing process, comprising:

a plurality of metal wire patterns, each including: ~~which include~~

main fine line patterns having a width of less than 1  $\mu\text{m}$ ;

main pad patterns;

connection pad patterns which electrically connect the main pad patterns to the fine line patterns; and

dummy fine line patterns having a sub-micron width; ~~said plurality of metal wire patterns being formed by patterning a same layer;~~ an area of the dummy fine line

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patterns, which are connected to the pad patterns, being formed to be less than 1% of a total area of said plurality of metal wire patterns according to a formula,

$$(d/(A_p+A_c+A+d) \times 100) < 1\%$$

and also being less than a value obtained by dividing an area of the main fine line patterns by said total area, which is represented by  $A_p+A_c+A+d$ , according to a formula,

$$(d/(A_p+A_c+A+d) < A/(A_p+A_c+A+d)$$

where, 'd' represents the area of the dummy fine line patterns, 'A<sub>p</sub>' represents an area of the main pad patterns, 'A<sub>c</sub>' represents an area of the connection pad patterns and 'A' represents the area of the main fine line patterns;

said pad patterns, said fine line patterns and said connection pad patterns of each metal wire pattern being formed in one layer and a width of said connection pad patterns being in a range between a width of said pad patterns and the width of said main fine line patterns.

16. (New) The semiconductor device as recited in claim 1, wherein each metal wire pattern further includes a dummy fine line pattern formed parallel with the main fine line pattern at a distance of approximately the width of said main fine line pattern.

17. (New) The semiconductor device as recited in claim 16, wherein each metal wire pattern further includes a large dummy pad pattern connected to the dummy fine line pattern.